PTO/SB/08 Equivalent

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			Application No.	10/712,212		
	STATEMENT BY APPLICANT		Filing Date	November 13, 2003		
			First Named Inventor	Michael Smith		
سرا			Art Unit	2815		
10	1 PE(Mylti)	ole sheets used when necessary)	Examiner	Allan R. Wilson		
	5	SHEET 1 OF 1	Attorney Docket No.	MICRON.271A		
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	NON PATENT LITERATURE DOCUMENTS					
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ¹			
(O de/		Sakao, et al. A STRAIGHT-LINE TRENCH ISOLATION AND TRENCH-GATE TRANSISTOR (SLIT) CELL FOR GIGA-BIT DRAMS; ULSI Device Development Laboratories, NEC Corporation; 1120, Shimokuzawa, Sagamihara, Kanagawa 229, Japan; "1993 Symposium on VLSI Technology, Digest of Technical Papers," Pages 19 and 20				

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Examiner Signature Q, 41/1/0/9

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Oraw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T¹ - Place a check mark in this area when an English language Translation is attached.

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